ABSTRACT OF THE DISCLOSURE

Bus-connected circuits are made to operate stably and at high speed. A cache memory for high-speed access and a DRAM for low-speed access are connected to a CPU by an address bus, control bus and data transfer bus. A switch is provided in the bus at a point between the cache memory and DRAM and the switch is opened at the time of high-speed access. Since bus length is essentially shortened at such time, the cache memory can be accessed stably at high speed. When the DRAM is accessed, the switch is closed.